AMENDMENTS TO THE CLAIMS

The embodiments of the invention in which an exclusive property or privilege is claimed are defined as follows:

1. (Currently Amended) A method of Edge-Node Interleave Sort for Leaching and Envelop(ENISLE),comprising:

mapping a circuit into a *V-E* plane, comprised of side, to transform a circuit information into said *V-E* plane which contains the information of node and edge information, wherein said *V* indicates nodes that represent components of said circuit and wherein said *E* indicates edges that represents nets of said circuit;

partitioning said *V-E* plane from a side V to form two node sets, wherein each node set includes at least one node;

determining whether *V-E* pairs distribution on said *V-E* plane is uniform or not, if said *V-E* pairs distribution is not uniformly distributed, then randomizing said *V-E* pairs on said *V-E* plane, otherwise performing the following steps for sequentially arranging the *V-E* pairs according to a magnitude respective to each said each node or said edge, thereby obtaining min-cut or/and ratio min-cut partitioning;

performing a first sorting step from an edge view based on a first side of said *V-E* plane;

performing a second sorting step from a node view based on a second side of said *V-E* plane;

performing a third sorting from said edge view based on a third side of said *V-E* plane; and

performing a fourth sorting step from said node view based on a fourth side of said *V-E* plane.

2. (Previously Amended) The method of claim 1, wherein said first side refers to a bottom side of said V-E plane.

3. (Previously Amended) The method of claim 1, wherein said second side refers to a right side of said V-E plane.

4. (Previously Amended) The method of claim 1, wherein said first side refers to a top side of said V-E plane.

5. (Previously Amended) The method of claim 1, wherein said first side refers to a left side of said V-E plane.

6. (Currently Amended) The method of claim 1, further comprising following steps after performing said fourth sorting:
    initializing a node set record;
    performing a fifth sorting step from said node view based on the second side;
    performing a sixth sorting step from said edge view based on said first side/third side;
    determining whether each said node set is still interchanged or not, if said node set is no longer interchanged, go back and perform said fifth sorting step, otherwise, perform a seventh sorting step from said node view based on said fourth side;
    determining whether each said node set is still interchangeinterchanged or not, if said node set is still interchanged, then perform said fifth sorting step for achieving an optimal min-cut or ratio min-cut partitioning.

7. (Previously Amended) The method of claim 6, wherein said first side refers to a bottom side of said V-E plane.

8. (Previously Amended) The method of claim 6, wherein said second side refers to a right side of said V-E plane.

9. (Previously Amended) The method of claim 6, wherein said first side refers to a top side of said V-E plane.

10. (Previously Amended) The method of claim 6, wherein said first side refers to a left side of said V-E plane.

11. (Currently Amended) A method for min-cut and/or ratio min-cut partitioning, comprising:
    mapping a circuit into a *V-E* plane, comprised of sides, to transform a circuit information into said *V-E* plane which contains the information of node and edge information, wherein said V

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indicates nodes that represent components of said circuit and wherein said E indicates edges that represents the nets of said circuit;

partitioning said *V-E* plane from a side V to form two node sets, wherein each node set includes at least one node;

performing the following steps for sequentially arranging of the *V-E* pairs according to a magnitude respective to each said node or said edge, thereby obtaining min-cut or/and ratio min-cut partitioning;

performing a first sorting step from an edge view based on a first side of said *V-E* plane;

performing a second sorting step from a node view based on a second side of said *V-E* plane;

performing a third sorting from said edge view based on a third side of said *V-E* plane; and

performing a fourth sorting step from said node view based on a fourth side of said *V-E* plane.

12. (Previously Amended) The method of claim 11, further comprising determining whether said V-E pairs distribution on said V-E plane is uniform or not, if said V-E pairs distribution is not uniformly distributed, then randomizing said V-E pairs on said V-E plane.

13. (Previously Amended) The method of claim 11, wherein said first side refers to a bottom side of said V-E plane.

14. (Previously Amended) The method of claim 11, wherein said second side refers to a right side of said V-E plane.

15. (Previously Amended) The method of claim 11, wherein said first side refers to a top side of said V-E plane.

16. (Previously Amended) The method of claim 11, wherein said first side refers to a left side of said V-E plane.

17. (Currently Amended) A method for min-cut and/or ratio min-cut partitioning, comprising:

mapping a circuit into a *V-E* plane, comprised of sides, to transform a circuit information into said *V-E* plane which contains the information of node and edge information, wherein said *V* indicates nodes that represent components of said circuit and wherein said *E* indicates edges that represents the nets of said circuit;

partitioning said *V-E* plane from a side V to form two node sets, wherein each node set includes at least one node;

determining whether *V-E* pairs distribution on said *V-E* plane is uniform or not, if said *V-E* pairs distribution is not uniformly distribute, then randomizing said *V-E* pairs on said *V-E* plane, otherwise performing the following steps for sequentially arranging of the *V-E* pairs according to a magnitude respective to each said node or said edge, thereby obtaining min-cut or/and ratio min-cut partitioning;

performing a first sorting step from an edge view based on a first side of said *V-E* plane;

performing a second sorting step from an node view based on a second side of said *V-E* plane;

performing a third sorting from said edge view based on a third side of said *V-E* plane;

performing a fourth sorting step from said node view based on a fourth side of said *V-E* plane;

initializing a node set node sets record;

starting a loop;

performing a fifth sorting step from said node view based on the second side and then recording said two node sets;

performing a sixth sorting step from said edge view based on said first side/third side and then recording said two node sets;

determining whether each said node set is still interchanged or not, if said each node set is no longer interchanged then go back to perform said fifth sorting step, otherwise, perform a seventh sorting step from said node view based on said fourth side;

determining whether each said node set is still interchanged or not, if said node set is still interchanged, then performing said fifth sorting step performing said fifth sorting step coming back to the start of the loop, for achieving an optimal min-cut or ratio min-cut partitioning.

18. (Withdrawn) A method for display data compression techniques by different light intensity and/or different patterns on a monochrome viewpoint, comprising:

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displaying (V, E) pairs on an initial V-E plane shown on a monitor screen to observe the said initial (V, E) pairs distributed condition, wherein said V indicates nodes that represent components of said circuit and wherein said E indicates edges that represents the nets of said circuits;

setting L nodes x W edges (V, E) pairs rectangle region to compose a block, wherein said L and W are integers;

defining the more (V, E) pairs in said block to be displayed by the relatively high light intensity to the less (V, E) pairs in said block; and

watching relatively large size of V-E plane or a whole V-E plane to said initial (V, E) plane on said monitor screen, wherein said exact (V, E) pairs positions still be held, thereby zooming in said V-E plane to watch detail local (V, E) pairs distributed condition, or zooming out to watch global (V, E) pairs distributed condition on said monitor screen.

19. (Withdrawn) A method for display data compression techniques by different light intensity and/or different patterns on a monochrome viewpoint, comprising:

displaying (V, E) pairs on an initial V-E plane shown on a monitor screen to observe the said initial (V, E) pairs distributed condition, wherein said V indicates nodes that represent components of said circuit and wherein said E indicates edges that represents the nets of said circuits;

setting L nodes x W edges (V, E) pairs rectangle region to compose a block, wherein said L and W are integers;

defining the less (V, E) pairs in said block to be displayed by the relatively high light intensity to the more (V E) pairs in said block; and

watching relatively large size of V-E plane or a whole V-E plane to said initial (V, E) plane on said monitor screen, wherein said exact (V, E) pairs positions still be held, thereby zooming in said V-E plane to watch detail local (V, E) pairs distributed condition, or zooming out to watch global (V, E) pairs distributed condition on said monitor screen.

20. (Withdrawn) A method for display data compression techniques by different color and/or different patterns on a monochrome viewpoint, comprising:

displaying (V, E) pairs on an initial V-E plane shown on a monitor screen to observe the said initial (V, E) pairs distributed condition, wherein said V indicates nodes that represent components of said circuit and wherein said E indicates edges that represents the nets of said circuits;

setting L nodes x W edges (V, E) pairs rectangle region to compose a block, wherein said L and W are integers;

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defining the more (V, E) pairs in said block to be displayed by the relatively bright color to the less (V, E) pairs in said block; and

watching relatively large size of V-E plane or a whole V-E plane to said initial (V, E) plane on said monitor screen., wherein said exact (V, E) pairs positions still be held, thereby zooming in said V-E plane to watch detail local (V, E) pairs distributed condition, or zooming out to watch global (V, E) pairs distributed condition on said monitor screen.

21. (Withdrawn) A method for display data compression techniques by different color and/or different patterns on a monochrome viewpoint, comprising:

displaying (V E) pairs on an initial V-E plane shown on a monitor screen to observe the said initial (V, E) pairs distributed condition, wherein said V indicates nodes that represent components of said circuit and wherein said E indicates edges that represents the nets of said circuits;

setting L nodes x W edges (V, E) pairs rectangle region to compose a block, wherein said L and W are integers;

defining the more (V, E) pairs in said block to be displayed by the relatively bright color to the less (V, E) pairs in said block; and

watching relatively large size of V-E plane or a whole V-E plane to said initial (V, E) plane on said monitor screen, wherein said exact (V, E) pairs positions still be held, thereby zooming in said V-E plane to watch detail local (V, E) pairs distributed condition, or zooming out to watch global (V, E) pairs distributed condition on said monitor screen.